



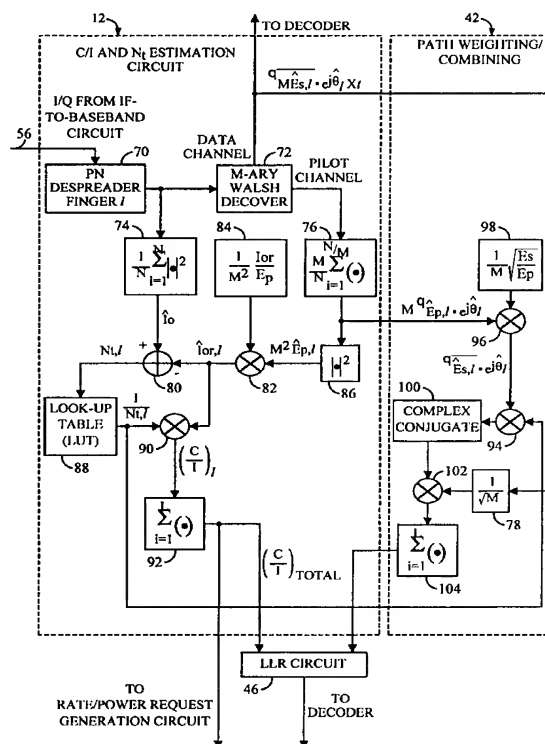
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(54) Title: SYSTEM AND METHOD FOR PROVIDING AN ACCURATE ESTIMATION OF RECEIVED SIGNAL INTERFERENCE FOR USE IN WIRELESS COMMUNICATIONS SYSTEMS

(57) Abstract

A system for providing an accurate interference value signal received over a channel and transmitted by an external transceiver. The system includes a first receiver section for receiving the signal, which has a desired signal component and an interference component. A signal extracting circuit extracts an estimate of the desired signal component from the received signal. A noise estimation circuit (12) provides the accurate interference value based on the estimate of the desired signal component and the received signal. A look-up table transforms the accurate noise and/or interference value to a normalization factor. A carrier signal-to-interference ratio circuit employs the normalization factor and the received signal to compute an accurate carrier signal-to-interference ratio estimate. Path-combining circuitry generates optimal path-combining weights based on the received signal and the normalization factor.



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SYSTEM AND METHOD FOR PROVIDING AN ACCURATE ESTIMATION OF RECEIVED SIGNAL INTERFERENCE FOR USE IN WIRELESS COMMUNICATIONS SYSTEMS

5

BACKGROUND OF THE INVENTION

I. Field of Invention:

This invention relates to communications systems. Specifically, the
10 present invention relates systems for estimating the interference spectral
density of a received signal in wireless code division multiple access (CDMA)
communications systems for aiding in rate and power control and signal
decoding.

15 II. Description of the Related Art:

Wireless communications systems are used in a variety of demanding
applications including search and rescue and business applications. Such
applications require efficient and reliable communications that can effectively
20 operate in noisy environments.

Wireless communications systems are characterized by a plurality of
mobile stations in communication with one or more base stations. Signals are
transmitted between a base station and one or more mobile stations over a
channel. Receivers in the mobile stations and base stations must estimate noise
25 introduced to the transmitted signal by the channel to effectively decode the
transmitted signal.

In a code division multiple access (CDMA) communications system,
signals are spread over a wide bandwidth via the use of a pseudo noise (PN)
spreading sequence. When the spread signals are transmitted over a channel,
30 the signals take multiple paths from the base station to the mobile station. The

signals are received from the various paths at the mobile station, decoded, and constructively recombined via path-combining circuitry such as a Rake receiver. The path-combining circuitry applies gain factors, called weights, to each decoded path to maximize throughput and compensate for path delays and fading.

Often, a communications system transmission includes pilot interval, a power control interval, and a data interval. During the pilot interval, the base station transmits a pre-established reference signal to the mobile station. The mobile station combines information from the received reference signal, i.e., pilot signal, and the transmitted pilot signal to extract information about the channel, such as channel interference and signal-to-noise (SNR) ratio. The mobile station analyzes the characteristics of the channel and subsequently transmits a power control signal to the base station in response thereto during a subsequent power control interval. For example, if the base station is currently transmitting with excess power given the current channel characteristics, the mobile station sends a control signal to the base station requesting that transmitted power level be reduced.

Digital communications systems often require accurate log-likelihood ratios (LLRs) to accurately decode a received signal. An accurate signal-to-noise ratio (SNR) measurement or estimate is typically required to accurately calculate the LLR for a received signal. Accurate SNR estimates require precise knowledge of the noise characteristics of the channel, which may be estimated via the use of a pilot signal.

The rate or power at which a base station or mobile station broadcasts a signal is dependant on the noise characteristics of the channel. For maximum capacity, transceivers in the base stations and mobile stations control the power of transmitted signals in accordance with an estimate of the noise introduced by the channel. If the estimate of the noise, i.e., the interference spectral density of different multipath components of the transmitted signal is inaccurate, the transceivers may broadcast with too much or too little power. Broadcasting with too much power may result in inefficient use of network resources,

resulting in a reduction of network capacity and a possible reduction in mobile station battery life. Broadcasting with too little power may result in reduced throughput, dropped calls, reduced service quality, and disgruntled customers.

Accurate estimates of the noise introduced by the channel are also
5 required to determine optimal path-combining weights. Currently, many CDMA telecommunications systems calculate SNR ratios as a function of the carrier signal energy to the total spectral density of the received signal. This calculation is suitable at small SNRs but becomes inaccurate at larger SNRs, resulting in degraded communications system performance.

10 In addition, many wireless CDMA communications systems fail to accurately account for the fact that some base stations that broadcast during the pilot interval do not broadcast during the data interval. As a result, noise measurements based on the pilot signal may become inaccurate during the data interval, thereby reducing system performance.

15 Hence, a need exists in the art for a system and method for accurately determining the interference spectral density of a received signal, calculating an accurate SNR or carrier signal-to-interference ratio, and determining optimal path-combining weights. There is a further need for a system that accounts for base stations that broadcast pilot signals during the pilot interval but do not
20 broadcast during the data interval.

SUMMARY OF THE INVENTION

25 The need in the art is addressed by the system for providing an accurate interference value for a signal received over a channel and transmitted by an external transceiver of the present invention. In the illustrative embodiment, the inventive system is adapted for use with a wireless code division multiple access (CDMA) communications system and includes a first receiver section for
30 receiving the signal, which has a desired signal component and an interference

and/or noise component. A signal extracting circuit extracts an estimate of the desired signal component from the received signal. A noise estimation circuit provides the accurate interference value based on the estimate of the desired signal component and the received signal. A look-up table transforms the accurate noise and/or interference value to a normalization factor. A carrier signal-to-interference ratio circuit employs the normalization factor and the received signal to compute an accurate carrier signal-to-interference ratio estimate. Path-combining circuitry generates optimal path-combining weights based on the received signal and the normalization factor.

In the illustrative embodiment, the system further includes a circuit for employing the accurate interference value to compute a carrier signal-to-interference ratio (C/I). The system further includes a circuit for computing optimal path-combining weights for multiple signal paths comprising the signal using the accurate interference value and providing optimally combined signal paths in response thereto. The system also includes a circuit for computing a log-likelihood value based on the carrier signal-to-interference ratio and the optimally combined signal paths. The system also includes a circuit for decoding the received signal using the log-likelihood value. An additional circuit generates a rate and/or power control message and transmits the rate and/or power control message to the external transceiver.

In a specific embodiment, the first receiver section includes downconversion and mixing circuitry for providing in-phase and quadrature signal samples from the received signal. The signal extracting circuit includes a pseudo noise despreaders that provides despread in-phase and quadrature signal samples from the in-phase and quadrature signal samples. The signal extracting circuit further includes a discovering circuit that separates data signals and a pilot signal from the despread in-phase and quadrature signal samples and provides a data channel output and a pilot channel output in response thereto. The signal extracting circuit further includes an averaging circuit for reducing noise in the pilot channel output and providing the estimate of the desired signal component as output in response thereto. The

noise estimation circuit includes a circuit for computing a desired signal energy value associated with the estimate, multiplying the desired signal energy value by a predetermined constant to yield a scaled desired signal energy value, and subtracting the scaled desired signal energy value from an estimate of the total energy associated with the received signal to yield the accurate interference value.

An alternative implementation of the noise estimation circuit includes a subtractor that subtracts the desired signal component from the pilot channel output and provides an interference signal in response thereto. The noise estimation circuit includes an energy computation circuit for providing the accurate interference value from the interference signal.

The accurate interference value is applied to a look-up table (LUT), which computes the reciprocal of the interference power spectral density, which corresponds to the accurate interference value. The reciprocal is then multiplied by the scaled desired signal energy value to yield a carrier signal-to-interference ratio (C/I) estimate that is subsequently averaged by an averaging circuit and input to a log likelihood ratio (LLR) circuit. The reciprocal is also multiplied by path-combining weights derived from the pilot channel output to yield normalized optimal path-combining weight estimates, which are subsequently scaled by a constant factor, averaged, and input to the LLR circuit, which computes the LLR of the received signal.

The circuit for computing optimal path-combining weights for each multiple signal path comprising the received signal includes a circuit for providing a scaled estimate of the complex amplitude of the desired signal component from an output of a pilot filter and a constant providing circuit. The scaled estimate is normalized by the accurate interference value. A conjugation circuit provides a conjugate of the scaled estimate, which is representative of the optimal path-combining weights.

The novel design of the present invention is facilitated by the noise estimation circuit that provides an accurate estimate of an interference component of the received signal. The accurate estimate of the interference

component results in a precise estimate of carrier signal-to-interference ratio, which facilitates optimal decoding of the received signal.

BRIEF DESCRIPTION OF THE DRAWINGS

5

Fig. 1 is a diagram of a telecommunications system of the present invention having an accurate interference energy computation circuit.

Fig. 2 is a more detailed diagram of the accurate interference energy computation circuit, log-likelihood ratio (LLR) circuit, and path-combining
10 circuit of Fig. 1 adapted for use with forward link transmissions.

Fig. 3 is a diagram of an accurate interference energy computation circuit optimized for reverse link transmission and including the path weighting and combining circuit and the LLR circuit of Fig. 2.

Fig. 4 is a diagram showing alternative embodiments of the accurate
15 interference energy estimation circuit and the maximal ratio path-combining circuit of Fig. 2.

Fig. 5 is a block diagram of a frame activity control circuit for improving estimates of interference energy and adapted for use with the accurate interference energy computation circuit of Fig. 2.

20 Fig. 6 is an exemplary timing diagram showing an active slot and idle slot.

Fig. 7 is an exemplary timing diagram showing a traffic channel signal, a pilot channel signal, a frame activity signal (FAC) (also known as a reverse power control channel), and idle channel skirts of the slots of Fig. 6.

25

DESCRIPTION OF THE INVENTION

While the present invention is described herein with reference to illustrative embodiments for particular applications, it should be understood
30 that the invention is not limited thereto. Those having ordinary skill in the art

and access to the teachings provided herein will recognize additional modifications, applications, and embodiments within the scope thereof and additional fields in which the present invention would be of significant utility.

Fig. 1 is a diagram of a telecommunications transceiver system 10 of the present invention having an accurate carrier signal-to-interference (C/I) and interference energy (N_i) computation circuit 12. The system 10 is adapted for use with a CDMA mobile station. In the present specific embodiment, signals received by the transceiver system 10 are received over a forward communications link between a base station (not shown) and the system 10. Signals transmitted by the transceiver system 10 are transmitted over a reverse communications link from the transceiver system 10 to the associated base station.

For clarity, many details of the transceiver system 10 have been omitted, such as clocking circuitry, microphones, speakers, and so on. Those skilled in the art can easily implement the additional circuitry without undue experimentation.

The transceiver system 10 is a dual conversion telecommunications transceiver and includes an antenna 14 connected to a duplexer 16. The duplexer 16 is connected to a receive path that includes, from left to right, a receive amplifier 18, a radio frequency (RF) to intermediate frequency (IF) mixer 20, a receive bandpass filter 22, a receive automatic gain control circuit (AGC) 24, and an IF-to-baseband circuit 26. The IF-to-baseband circuit 26 is connected to a baseband computer 28 at the C/I and N_i estimation circuit 12.

The duplexer 16 is also connected to a transmit path 66 that includes a transmit amplifier 30, an IF-to-RF mixer 32, a transmit bandpass filter 34, a transmit AGC 36, and a baseband-to-IF circuit 38. The transmit baseband-to-IF circuit 38 is connected to the baseband computer 28 at an encoder 40.

The C/I and N_i estimation circuit 12 in the baseband computer 28 is connected to a path weighting and combining circuit 42, a rate/power request generation circuit 44, and a log-likelihood ratio (LLR) circuit 46. The LLR circuit 46 is also connected to the path weighting and combining circuit 42 and

a decoder 48. The decoder 48 is connected to a controller 50 that is also connected to the rate/power request generation circuit 44 and the encoder 40.

The antenna 14 receives and transmits RF signals. A duplexer 16, connected to the antenna 14, facilitates the separation of receive RF signals 52 from transmit RF signals 54.

RF signals 52 received by the antenna 14 are directed to the receive path 64 where they are amplified by the receive amplifier 18, mixed to intermediate frequencies via the RF-to-IF mixer 20, filtered by the receive bandpass filter 22, gain-adjusted by the receive AGC 24, and then converted to digital baseband signals 56 via the IF-to-baseband circuit 26. The digital baseband signals 56 are then input to a digital baseband computer 28.

In the present embodiment, the receiver system 10 is adapted for use with quadrature phase shift-keying (QPSK) modulation and demodulation techniques, and the digital baseband signals 56 are quadrature amplitude modulation (QAM) signals that include both in-phase (I) and quadrature (Q) signal components. The I and Q baseband signals 56 represent both pilot signals and data signals transmitted from a CDMA telecommunications transceiver such as a transceiver employed in a base station.

In the transmit path 66, digital baseband computer output signals 58 are converted to analog signals via the baseband-to-IF circuit 38, mixed to IF signals, filtered by the transmit bandpass filter 34, mixed up to RF by the IF-to-RF mixer 32, amplified by the transmit amplifier 30 and then transmitted via the duplexer 16 and the antenna 14.

Both the receive and transmit paths 64 and 66, respectively, are connected to the digital baseband computer 28. The digital baseband computer 28 processes the received baseband digital signals 56 and outputs the digital baseband computer output signals 58. The baseband computer 28 may include such functions as signal to voice conversions and/or vice versa.

The baseband-to-IF circuit 38 includes various components (not shown) such as digital-to-analog converters (DACs), mixers, adders, filters, shifters, and

local oscillators. The baseband computer output signals 58 include both in-phase (I) and quadrature (Q) signal components that are 90° out of phase. The output signals 58 are input to digital-to-analog converters (DACs) in the analog baseband-to-IF circuit 38, where they are converted to analog signals that are
5 then filtered by lowpass filters in preparation for mixing. The phases of the output signals 58 are adjusted, mixed, and summed via a 90° shifter (not shown), baseband-to-IF mixers (not shown), and an adder (not shown), respectively, included in the baseband-to-IF circuit 38.

The adder outputs IF signals to the transmit AGC circuit 36 where the
10 gain of the mixed IF signals is adjusted in preparation for filtering via the transmit bandpass filter 34, mixing up to RF via the IF-to-transmit mixer 32, amplifying via the transmit amplifier 20, and eventual radio transmission via the duplexer 16 and the antenna 14.

Similarly, the IF-to-baseband circuit 26 in the receive path 64 includes
15 circuitry (not shown) such as analog-to-digital (ADC) converters, oscillators, and mixers. A received gain-adjusted signals output from the receive AGC circuit 24 are transferred to the IF-to-baseband circuit 26 where they are mixed to baseband via mixing circuitry and then converted to digital signals via analog-to-digital converters (ADCs).

Both the baseband-to-IF circuit 38 and the IF-to-baseband circuit 36
20 employ an oscillator signal provided via a first oscillator 60 to facilitate mixing functions. The receive RF-to-IF mixer 20 and the transmit IF-to-RF mixer 32 employ an oscillator signal input from a second oscillator 62. The first and second oscillators 60 and 6, respectively, may be implemented as phase-locked
25 loops that derive output signals from a master reference oscillator signal.

Those skilled in the art will appreciate that other types of receive and transmit paths 64 and 66 may be employed instead without departing from the scope of the present invention. The various components such as amplifiers 18 and 30, mixers 20 and 32, filters 22 and 34, AGC circuits 24 and 36, and
30 frequency conversion circuits 26 and 38 are standard components and may

easily be constructed by those having ordinary skill in the art and access to the present teachings.

In the baseband computer 28, the received I and Q signals 56 are input to the C/I and N_t estimation circuit 12. The C/I and N_t estimation circuit 12 accurately determines the interference energy of the I and Q signals 56 based on the pilot signal and determines a carrier signal-to-interference ratio in response thereto. The carrier signal-to-interference ratio (C/I) is similar to signal-to-noise ratio (SNR) and is the ratio of the energy of the received I and Q signals 56 less interference and noise components to the interference energy of the received I and Q signals 56. Conventional C/I estimation circuits often fail to accurately estimate the multipath interference energy.

The C/I and N_t estimation circuit 12 outputs a C/I signal to the rate/power request generation circuit 44 and the LLR circuit 46. The C/I and N_t estimation circuit 12 also outputs the reciprocal of the interference energy ($1/N_t$), a despread and deconvolved data channel signal, and a despread and deconvolved pilot channel signal to the path weighting and combining circuit 42. The despread and deconvolved data channel signal is also provided to the decoder 48 where it is decoded and forwarded to the controller 50. At the controller 50, the decoded signal is processed to output voice or data, or to generate a reverse link signal for transfer to the associated base station (not shown).

The path weighting and combining circuit 42 computes optimal ratio path-combining weights for multipath components of the received data signal corresponding to the data channel signal, weights the appropriate paths, combines the multiple paths, and provides the summed and weighted paths as a metric to the LLR circuit 46.

The LLR circuit 46 employs metrics from the path weighting and combining circuit 42 with the C/I estimation provided by the C/I and N_t estimation circuit 12 to generate an optimal LLR and soft decoder decision values. The optimal LLR and soft decoder decision values are provided to the decoder 48 to facilitate decoding of the received data channel signals. The

controller 50 then processes the decoded data channel signals to output voice or data via a speaker or other device (not shown). The controller 50 also controls the sending of speech signals and data signals from an input device (not shown) to the encoder 40 in preparation for transmission.

5 The rate/power request generation circuit 44 generates a rate control or power fraction request message based on the C/I signal input from the C/I and N_t estimation circuit 12. The rate/power request generation circuit 44 compares the C/I with a set of predetermined thresholds. The rate/power request generation circuit 44 generates a rate request or power control message
10 based on the relative magnitude of the C/I signal with respect to the various thresholds. The exact details of the rate/power request generation circuit 44 are application-specific and easily determined and implemented by those ordinarily skilled in the art to suit the needs of a given application.

 The resulting rate control or power fraction request message is then
15 transferred to the controller 50. The controller 50 prepares the power fraction request message for encoding via the encoder 40 and eventual transmission to the associated base station (not shown) over a data rate request channel (DRC) via the transmit path 66, duplexer 16 and antenna 14. When the base station receives the rate control or power fraction request message, the base station
20 adjusts the rate and/or power of the transmitted signals accordingly.

 The accurate C/I and N_t estimates from the C/I and N_t estimation circuit 12 improve the performance of the rate/power request generation circuit 44 and improve the performance of the decoder 48, thereby improving the throughput and efficiency of the transceiver system 10 and associated
25 telecommunications system.

 Fig. 2 is a more detailed diagram of the accurate C/I and N_t estimation circuit 12, LLR circuit 46, and path-combining circuit 42 of Fig. 1 adapted for use with forward link transmissions.

 The C/I and N_t estimation circuit 12 includes, from left to right and top
30 to bottom, a pseudo noise (PN) despreader 70, an M-ary Walsh decoder circuit 72, a total received signal energy (I_o) computation circuit 74, a first constant

circuit 84, a pilot filter 76, a subtractor 80, a first multiplier 82, a pilot energy calculation circuit 86, a look-up table (LUT) 88, a second multiplier 90, and a C/I accumulation circuit 92. In the C/I and N_t estimation circuit 12, the pseudo noise (PN) despreaders 70 receives the I and Q signals 56 from the IF-to-baseband circuit 26 of Fig. 1. The PN despreaders 70 provides input, in parallel, to the M-ary Walsh decoder circuit 72 and the I_o computation circuit 74. The M-ary Walsh decoder circuit 72 provides input to the pilot filter 76 and to a constant divider circuit 78 in the path weighting and combining circuit 42.

The output of the energy computation circuit 74 is connected to a positive terminal of the subtractor circuit 80. A negative terminal of the subtractor circuit 80 is connected to an output terminal of a first multiplier 82. A first input of the first multiplier 82 is connected to an output of the first constant circuit 84. A second input of the first multiplier 82 is connected to an output of the pilot energy calculation circuit 86. The pilot filter 76 provides input to the pilot energy calculation circuit 86.

An output of the subtractor 80 is connected to the look-up table (LUT) 88. An output of the LUT 88 is connected, in parallel, to a first input of the second multiplier 90 and a first input of a third multiplier 94 in the path weighting and combining circuit 42. A second input of the second multiplier 90 is connected to the output of the first multiplier 82. An output of the second multiplier 90 is connected to the C/I accumulator circuit 92, the output of which provides input to the LLR circuit 46.

The path weighting and combining circuit 42 includes a second constant generation circuit 98, a fourth multiplier 96, the third multiplier 94, the constant divider circuit 78, a complex conjugate circuit 100, a fifth multiplier 102, and a path accumulator circuit 104. In the path weighting and combining circuit 42, a first terminal of the fourth multiplier 96 is connected to the output of the pilot filter 76, which is also connected to an input of the pilot energy calculation circuit 86 in the C/I and N_t estimation circuit 12. A second terminal of the fourth multiplier 96 is connected to the second constant generation circuit 98. An output of the fourth multiplier 96 is connected to a second input of the third

multiplier 94. The output of the third multiplier 94 provides input to the complex conjugate circuit 100. The output of the complex conjugate circuit 100 is connected to a first input of the fifth multiplier 102. An output of the constant divider circuit 78 is connected to a second input of the fifth multiplier 102. An output of the fifth multiplier 102 is connected to an input of the path accumulator circuit 104. The output of the path accumulator circuit 104 is connected to a second input of the LLR circuit 46. The output of the LLR circuit is connected to an input of a decoder (see 48 of Fig. 1).

In operation, the PN despreader 70 receives the I and Q signals and despreads L fingers, i.e., paths (*l*). The PN despreader 70 despreads the I and Q signals using an inverse of the pseudo noise sequence used to spread the I and Q signals before transmission over the channel. The construction and operation of the PN despreader 70 is also well known in the art.

Despread signals are output from the PN despreader 70 and input to the M-ary Walsh decoder 72 and the I_o computation circuit 74. The I_o computation circuit 74 computes the total received energy (I_o) per chip, which includes both a desired signal component and an interference and noise component. The I_o computation circuit provides an estimate (\hat{I}_o) of I_o in accordance with the following equation:

20

$$\hat{I}_o = \frac{1}{N} \sum_{i=1}^N |\bullet|^2, \quad [1]$$

where N is the number of chips per pilot burst and is 64 in the present specific embodiment and \bullet represents the received despread signal output from the PN despreader 70.

Those skilled in the art will appreciate that the I_o may be computed before despreading by the PN despreader 70 without departing from the scope of the present invention. For example, the I_o computation circuit 74 may receive direct input from the I and Q signals 56 instead of input provided by the PN

despreader 70, in which case an equivalent estimate of I_o will be provided at the output of the I_o computation circuit 74.

The M-ary Walsh decoder circuit 72 discovers orthogonal data signals, called data channels, and pilot signals, called the pilot channel, in accordance with methods known in the art. In the present specific embodiment, the orthogonal data signals correspond to one data channel (s) that is represented by the following equation:

$$s = \sqrt{M \hat{E}_{s,l}} \cdot e^{j\hat{\theta}_l} X_l, \quad [2]$$

10

where M is the number of chips per Walsh symbol, $\hat{E}_{s,l}$ is the modulation symbol energy of the l^{th} multipath component, $\hat{\theta}_l$ is the phase of the data channel s, and X_l is the information-baring component of the data channel s.

15 The discovered data channel represented by equation (2) is provided to the decoder (see 48 of Fig. 1) and to the constant divider circuit 78 of the path weighting and combining circuit 42.

While the present invention is adapted for use with signals comprising various Walsh codes, the present invention is easily adaptable for use with other types of codes by those ordinarily skilled in the art.

20

The pilot channel is input to the pilot filter 76. The pilot filter 76 is an averaging filter that acts as a lowpass filter, which removes higher frequency noise and interference components from the pilot channel. The output of the pilot filter 76 (p) is represented by the following equation:

25

$$p = M \sqrt{\hat{E}_{p,l}} \cdot e^{j\theta_l}, \quad [3]$$

where M is the number of chips per Walsh symbol, $\hat{E}_{p,l}$ is the pilot chip energy of the l^{th} multipath component, and θ_l is the phase of the filtered pilot channel

30 p.

An estimate of the energy of the filtered pilot channel p is computed via the pilot energy calculation circuit 86, which is a square of the complex amplitude of the filtered pilot channel p represented by equation (3). The square of the complex amplitude of the filtered pilot channel p is multiplied by
 5 a predetermined scale factor c represented by the following equation:

$$c = \frac{1}{M^2} \frac{I_{or}}{E_p}, \quad [4]$$

where I_{or} is the received energy of the desired signal, i.e., is equivalent to I_o less
 10 noise and interference components. E_p is the pilot chip energy. The scale factor c is a known forward link constant in many wireless communications systems.

The scale factor c is multiplied by the energy of the filtered pilot signal p via the first multiplier 82 to yield an accurate estimate $\hat{I}_{or,l}$ of the energy of the
 15 received desired signal (I_o less noise and interference components) associated with the l^{th} multipath component of the received signals 56.

The accurate estimate $\hat{I}_{or,l}$ is subtracted from the estimate of I_o via the subtractor 80 to yield an accurate measurement of the interference energy ($N_{i,l}$) associated with the l^{th} multipath component. $N_{i,l}$ is then provided to the LUT
 20 88, which outputs the reciprocal of $N_{i,l}$ to the third multiplier 94 in the path weighting and combining circuit 42 and to the first input of the second multiplier 90. The second input of the second multiplier 90 is connected to the output of the first multiplier 82, which provides $\hat{I}_{or,l}$ at the second input terminal of the second multiplier 90. The second multiplier 90 outputs an
 25 accurate estimate of the carrier signal-to-interference ratio $(C/I)_l$ associated with the l^{th} multipath component in accordance with the following equation:

$$\left(\frac{C}{I}\right)_l = \frac{\hat{I}_{or,l}}{N_{i,l}}. \quad [5]$$

The accurate C/I value is then accumulated over L paths in the received signal via the C/I accumulator circuit 92. The accumulated C/I values are then provided to the LLR circuit 46 and to the rate/power request generation circuit
 5 (see 44 of Fig. 1).

In the path weighting and combining circuit 42, the fourth multiplier 96 multiplies the filtered pilot signal p by a constant k provided by the second constant generation circuit 98. The constant k is computed in accordance with the following equation:

10

$$k = \frac{1}{M} \sqrt{\frac{E_s}{E_p}}, \quad [6]$$

where E_s is the modulation symbol energy, E_p is the pilot symbol energy, and M is the number of Walsh symbols per chip as mentioned above. The ratio of E_s to
 15 E_p is often a known constant for both reverse link and forward link transmissions.

The output of the fourth multiplier 96 provides an estimate of the channel coefficient ($\hat{\alpha}$) described by the following equation:

20

$$\hat{\alpha} = \sqrt{\hat{E}_{s,l}} \cdot e^{j\hat{\theta}_l}, \quad [7]$$

where $\hat{E}_{s,l}$ is an estimate of the modulation symbol energy of the l^{th} multipath component, $\hat{\theta}_l$ is an estimate of the phase of the pilot signal. The channel $\hat{\alpha}$ is a scaled estimate of the complex amplitude of the output of the pilot filter 76.

25

The channel estimate is then multiplied by the reciprocal of the interference energy $N_{t,l}$ associated with the l^{th} multipath component by the third multiplier 94. The interference energy $N_{t,l}$ includes both interference and noise components. The complex conjugate circuit 100 then computes the conjugate of the output of the third multiplier 94, which represents maximal ratio path-

combining weights. The maximal ratio path-combining weights are then multiplied by the corresponding data symbol output from the divider circuit 78 via the fifth multiplier 102. The data symbol (d) is represented by the following equation:

5

$$d = \sqrt{\hat{E}_{s,l}} \cdot e^{j\hat{\theta}_l} X_l, \quad [8]$$

where the variables are as given for equations (2) and (7).

The output of the fifth multiplier 102 represents optimally weighted data signals that are then accumulated over the L paths that comprise the signals via the path combiner circuit 104. The resulting optimally combined data signals are provided to the LLR circuit 46, which facilitates the calculation of optimal soft decoder inputs to the decoder (see 48 of Fig. 1).

Those skilled in the art will appreciate that the constants c and k provided by the first constant generation circuit 84 and the second constant generation circuit 98, respectively, may be constants or variables other than those represented by equations (3) and (6) without departing from the scope of the present invention.

Fig. 3 is a diagram of an accurate interference energy computation circuit 110 optimized for reverse link transmission and including the path weighting and combining circuit 42 and the LLR circuit 46 of Fig. 2.

The operation of the interference energy computation circuit 110 is similar to the operation of the C/I and N_t estimation circuit 12 of Fig. 2 with the exception of the calculation of N_t . The interference energy computation circuit 110 includes the PN despreaders 70, the M-ary Walsh decoder circuit 72, and the pilot filter 76. The M-ary Walsh decoder circuit 72 decodes, i.e., extracts the pilot channel and the data channel from the despread I and Q signal samples output from the PN despreaders 70.

In the interference energy computation circuit 110, the pilot channel is provided to a positive input of a pilot subtractor circuit 112 and to the pilot

filter 76. The pilot filter 76 suppresses noise and interference components in the pilot channel and provides a filtered pilot signal to a negative input of the pilot subtraction circuit 112. The pilot subtractor circuit 112 subtracts the pilot channel from the filtered pilot channel and outputs a signal representative of the interference and noise per symbol introduced by the channel between the transmitting base station (not shown) and the transceiver system (see 10 of Fig. 1) in which the interference energy computation circuit 110 is employed. The energy ($N_{t,l}$) of the interference and noise signal for each symbol computed via an interference energy computation circuit 114 in accordance with the following equation:

$$N_{t,l} = \frac{M}{N} \sum_{i=1}^{N/M} |\bullet|^2, \quad [9]$$

where M is the number of chips per Walsh symbol, N is the number of chips (64 chips) in the pilot burst, and \bullet is the output of the pilot subtractor circuit 112.

The interference energy computation circuit 110 is employed when the constant value c provided by the first constant generation circuit 84 of Fig. 2 is not known. This is the case with many reverse link applications.

Fig. 4 is a diagram showing alternative embodiments 120 and 122 of the accurate interference energy estimation circuit and the maximal ratio path-combining circuit of Fig. 2, respectively, and adapted for use with a forward link. The alternative C/I and N_t estimation circuit 120 includes a pilot fingers filter 124 connected, in parallel, to pilot energy calculation circuit 86 and to an input of a pilot signal multiplier 126. The output of the pilot energy calculation circuit 86 is connected, in parallel, to the LUT 88 and to an input of a pilot energy signal multiplier 128.

An output of the LUT 88 is connected, in parallel, to another input of the a pilot energy signal multiplier 128 and to another input of the pilot signal multiplier 126. The output of the pilot energy signal multiplier 128 is input to a C/I path accumulation circuit 130. An output of the C/I path accumulation

circuit 130 is connected, in parallel, to an input of the rate/power generation circuit 44 of Fig. 1 and to an input of an generalized dual maxima circuit 132.

An output of the pilot signal multiplier 126 is connected to an input of a dot product circuit 134. Another input of the dot product circuit 134 is connected to an output of the M-ary Walsh decoder circuit 72 of Fig. 3. An output of the dot product circuit 134 is connected to an input of an I and Q signal demultiplexer (DEMUX) 136. The I and Q DEMUX 136 provides a quadrature output (Y_Q) and an in-phase output (Y_I) of the I and Q signal DEMUX 136 are connected to an input of the generalized dual maxima circuit 138. An in-phase metric (m_I) and a quadrature metric (m_Q) of the generalized dual maxima circuit 132 are connected to the LLR circuit (see 46 of Figs. 1, 2, and 3). The I and Q DEMUX 136 provides a quadrature output (Y_Q) and an in-phase output (Y_I) of the I and Q signal DEMUX 136 are connected to an input of the generalized dual maxima circuit 138.

In operation, the pilot fingers filter 124 receives a despread pilot signal from the output of the M-ary Walsh decoder circuit 72 of Fig. 3 and outputs a filtered signal (p) in accordance with the following equation:

$$p = \frac{P_l}{\sqrt{I_0}}, \quad [10]$$

where P_l is a pilot signal associated with the l^{th} multipath component of the received pilot signal, and I_0 is the total received energy per chip as defined by the following equation:

$$I_0 = I_{or,l} + N_{l,l}, \quad [11]$$

where $N_{l,l}$ represents, as previously mentioned, the interference and noise component associated with the l^{th} multipath component of the received signal, and $I_{or,l}$ represents the energy of the desired component of the received signal associated with the l^{th} multipath component.

The filtered signal p is input to the pilot energy calculation circuit 86 where the magnitude of the signal p is squared and output to the LUT 88. The LUT 88 is adjusted to subtract the squared signal p^2 from 1 and then invert the result to yield the following equation:

5

$$\frac{1}{1 - \frac{|P_l|^2}{I_0}} = \frac{I_0}{I_0 - |P_l|^2} = \frac{I_0}{N_{t,l}}, \quad [12]$$

where P_l and I_0 are as given for equations (10) and (11). $N_{t,l}$, as mentioned previously, represents the energy associated with an interference and noise component of the received signal associated with the l^{th} multipath component. $|P_l|^2$ provides an accurate estimate of $I_{0,l}$.

The resulting output of the LUT 88 is multiplied by the output of the pilot energy computation circuit 86 via the pilot energy signal multiplier 128 to yield an accurate C/I value for the l^{th} multipath component of the signal received by the system 20 of Fig. 1. The C/I values are added over the L multipaths comprising the received signal via the C/I path accumulation circuit 130. The C/I path accumulation circuit 130 provides an accurate estimate of the total C/I to the rate/power request generation circuit 44 of Fig. 1 and to the dual maxima computation circuit 132.

The pilot signal multiplier 126 multiplies the output of the pilot fingers filter 124 with the output of the LUT 88 to yield the following output (y):

$$y = \frac{P_l \sqrt{I_0}}{N_{t,l}}, \quad [13]$$

where the variables are as given for equation (12).

The output of the pilot signal multiplier 126 as given in equation 13 is provided to the dot product circuit 134. The dot product circuit 134 also receives as input a data signal (d) from the M-ary Walsh decoder circuit 72 of

Fig. 2. In the present embodiment, the data signal d is represented by the following equation:

$$d = \frac{X_l}{\sqrt{I_0}}, \quad [14]$$

5 where X_l is a quadrature amplitude modulation (QAM) signal associated with the l^{th} multipath component of the signal received by the system 20 of Fig. 1, and I_0 is as given in equation (11).

The system of Fig. 4 implements a similar algorithm as the system of Fig. 2 with the exception that the system of Fig. 4 shows scaling due to automatic gain control circuitry (see Fig. 1) explicitly. The system of Fig. 4 also shows the LUT 88 used to convert $(I_{or,l})/(I_0)$ to $(I_{or,l})/(N_{t,l})$ and to the reciprocal of $(N_{t,l})/(I_0)$ without explicitly computing I_0 as in Fig. 2. $(I_{or,l})/(I_0)$ is approximately equal to $(|P_l|^2)/(I_0)$ as output from the pilot energy calculation circuit 86 of Fig. 4 and equals E_p/I_0 if $E_p/I_{or} = 1$, where E_p is the pilot symbol energy as described above.

15 The dot product circuit 134 takes the dot produce of the signal d with the signal y , which are defined in equations (14) and (13), respectively, and provides an output signal (Y) in accordance with the following equation:

$$Y = \sum_{l=1}^L \frac{X_l P_l^*}{N_{t,l}} = Y_I + iY_Q, \quad [15]$$

20

where L is the total number of multipaths; l is a counter and represents a particular l path of the L multipaths; Y_I represents an in-phase component of the received data signal, and Y_Q represents an imaginary quadrature component of the received data signal. The other variables, i.e., X_l , P_l , and $N_{t,l}$, are as given for equations (13 and (14).

25

The DEMUX 136 selectively switches I (Y_I) and Q (Y_Q) components of the output Y defined by equation (15) onto separate paths that are provided to

the generalized dual maxima circuit 132 that outputs metrics \hat{m}_I and \hat{m}_Q , respectively, in response thereto to the LLR circuit 46 of Fig. 1.

All circuit components and modules employed to construct the present invention such as those employed in the system of Fig. 4 are easily constructed
5 by those having ordinary skill in the art.

Fig. 5 is a block diagram of a frame activity control (FAC) circuit 140 for improving estimates of interference energy (N_i) and adapted for use with the accurate C/I and N_t estimation circuit 12 of Fig. 2.

With reference to Figs. 2 and 5, the FAC circuit 140 can be inserted in the
10 C/I and N_t estimation circuit 12 of Fig. 2 at the input of the LUT 88. The FAC circuit 140 receives $N_{t,i}$ from the output of the subtractor circuit 80 and the data channel output from the M-ary Walsh Decoder 72, and the output of the first multiplier 82 and outputs a new estimate of $N_{t,i}$, i.e., N_i^{Data} , which is an interference (including noise) estimate revised for the fact that some base
15 stations broadcast during the pilot interval and do not broadcast during the data interval. Base stations that broadcast during the pilot interval contribute to the noise and interference associated with the channel and measured via the pilot signal. If some base stations do not broadcast during the data interval but broadcast during the pilot interval, the estimate of the channel noise and
20 interference based on the pilot interval will be too large, i.e., $N_{t,data} < N_{t,pilot}$ and $(C/I)_{data} < (C/I)_{pilot}$.

In accordance with the teachings of the present invention, waveforms broadcast by base stations include a frame activity bit (FAC bit). The FAC bit indicates to a mobile station, such as the system 10 of Fig. 1 whether or not the
25 traffic channel of the associated pilot signal will be transmitting during the half frame following the next half frame. If the FAC bit is set to a logical 1 for example, the forward traffic channel may be inactive. If the FAC bit is clear, i.e., corresponds to a logical 0, the corresponding forward channel is inactive. The FAC bit transmitted during half-frame n for the i^{th} base station, i.e., $FAC_i(n)$

specifies the forward data channel activity for the next frame, i.e., half frame (n+2).

Use of the FAC bit improves C/I estimates in communications systems where some base stations broadcast during the pilot interval and not during the data interval. As a result, use of the FAC bit results in superior data rate control as implemented via the rate/power request generation circuit 44 of Fig. 1. Use of the FAC bit also helps to ensure that forward data channel transmissions of up to 8 slots beginning with half-frame n+1 and based on data rate control messages accounting for base station inactivity via the FAC bits are valid.

The FAC circuit 140 subtracts the interference contributions from the base stations that will not be broadcasting during the data interval in accordance with the following equation.

$$N_{t,i}^{Data} = N_{t,i}^{Pilot} - \sum_{j: j \neq i, FAC[j]=0} \hat{I}_{or,j} , \quad [16]$$

where i is the index of the base station, i.e., sector for which $N_{t,i}^{Data}$ is being estimated. j is a counter that is incremented for each base station counted. $N_{t,i}^{Data}$ represents the interference energy for the l^{th} multipath component and associated with the data transmission for the j^{th} base station. Similarly, $N_{t,i}^{Pilot}$ represents the interference energy for the l^{th} multipath component and associated with the pilot transmission for the j^{th} base station. $\hat{I}_{or,j}$ is the energy of the desired signal component received from the j^{th} base station.

With access to the present teachings, those ordinarily skilled in the art can easily construct the FAC circuit 140 without undue experimentation.

During the pilot interval and while the interference energy N_t is being estimated, all base stations in communication with the transceiver system 10 of Fig. 1 are transmitting at full power. If a certain base station is idle during the data intervals preceding and following a pilot interval, then in the presence of a

large multipath spread, the interference from the base station may not be received during the entire duration of the pilot signal from another base station. To avoid a resulting inaccuracy in the estimation of N_r , the base station transmits an idle skirt signal before and after pilot bursts and during idle data
5 intervals. The length of the idle skirt signal is longer than the anticipated multipath spread associated with the channel. In a preferred embodiment, the length of the idle skirt signal is configurable from a minimum length of zero to a maximum length of 128 chips.

Fig. 6 is an exemplary timing diagram showing an active slot 150 and an
10 idle slot 152. Pilot skirts 154 are shown before and after a first pilot burst 156 and during idle slot 152. The first pilot burst 156 corresponds to a second pilot burst 158 during the active slot 150.

FAC signals 164, i.e., reverse power control channel (RPC) signals are also shown before and after a third pilot burst 160 in the idle slot 152 and a
15 corresponding fourth pilot burst 162 in the active slot 150. .

Fig. 7 is an exemplary timing diagram showing a traffic channel signal 170, a pilot channel signal 172, a frame activity signal 178 (FAC), and idle channel skirt signal 180 of the slots of Fig. 6.

Thus, the present invention has been described herein with reference to a
20 particular embodiment for a particular application. Those having ordinary skill in the art and access to the present teachings will recognize additional modifications, applications, and embodiments within the scope thereof.

It is therefore intended by the appended claims to cover any and all such applications, modifications and embodiments within the scope of the present
25 invention.

What Is Claimed Is:

CLAIMS

1. A system for providing an accurate noise and/or interference value
2 for a signal received over a wireless channel and transmitted by an external
transceiver comprising:
4 a first code division multiple access receiver section for receiving said
signal, said received signal having a desired signal component and an
6 interference and/or noise component;
a signal extracting circuit for extracting an estimate of said desired signal
8 component from said received signal;
a noise estimation circuit for providing said accurate noise and/or
10 interference value based on said estimate of said desired signal component and
said received signal;
12 a look-up table for transforming said accurate noise and/or interference
value to a normalization factor;
14 a carrier signal-to-interference ratio circuit for employing said
normalization factor and said received signal to generate an accurate carrier
16 signal-to-interference ratio estimate; and
path-combining circuitry for generating optimal path-combining weights
18 based on said received signal and said normalization factor.
2. The system of Claim 1 further including means for employing said
2 accurate interference value to compute a carrier signal-to-interference ratio.
3. The system of Claim 2 further including means for computing optimal
2 path-combining weights for multiple signal paths comprising said signal using
said accurate noise and/or interference value and providing optimally
4 combined signal paths in response thereto.

4. The system of Claim 3 further including means for computing a log-likelihood value based on said carrier signal-to-interference ratio and said optimally combined signal paths.

5. The system of Claim 4 further including means for decoding said received signal using said log-likelihood value.

6. The system of Claim 2 further including means for generating a rate and/or power control message and transmitting said rate and/or power control message to said external transceiver.

7. The system of Claim 1 wherein said first receiver section includes downconversion and mixing circuitry for providing in-phase and quadrature signal samples from said received signal.

8. The system of Claim 7 wherein said signal extracting circuit includes a pseudo noise despreader for providing despread in-phase and quadrature signal samples from said in-phase and quadrature signal samples.

9. The system of Claim 8 wherein said signal extracting circuit further includes a discovering circuit for separating a pilot signal and data signals from said despread in-phase and quadrature signal samples and providing a data channel output and a pilot channel output in response thereto.

10. The system of Claim 9 wherein said data channel output is described by the following equation:

$$s = \sqrt{M \hat{E}_{s,l}} \cdot e^{j\hat{\theta}_l} X_t,$$

where s represents the data channel, M is the number of chips per Walsh symbol; $\hat{E}_{s,l}$ is a modulation symbol energy of an l^{th} multipath component of

6 said data channel; $\hat{\theta}_l$ is a phase of the data channel s ; and X_l is an information-
 6 baring component of said data channel s .

11. The system of Claim 9 wherein said signal extracting circuit further
 2 includes an averaging circuit for reducing noise in said pilot channel output
 and providing said estimate of said desired signal component as output in
 4 response thereto.

12. The system of Claim 11 wherein said estimate of said desired signal
 2 component is described by the following equation:

$$p = M \sqrt{\hat{E}_{p,l}} \cdot e^{j\theta_l}$$

4 where p represents said estimate; M is the number of chips per Walsh symbol;
 $\hat{E}_{p,l}$ is a pilot chip energy of an l^{th} multipath component of said estimate p ; and
 6 θ_l is a phase of said estimate p .

13. The system of Claim 11 wherein said noise estimation circuit
 2 includes a circuit for computing an energy value associated with said estimate,
 multiplying said energy value by a predetermined constant to yield a scaled
 4 energy value, and subtracting said scaled energy value from an estimate of the
 total energy associated with said received signal to yield said accurate noise
 6 and/or interference value.

14. The system of Claim 13 wherein said predetermined constant is
 2 described by the following equation:

$$c = \frac{1}{M^2} \frac{I_{or}}{E_p}$$

4 where c represents said predetermined constant; I_{or} is the received energy of
 said desired signal component; and E_p is a pilot chip energy.

15. The system of Claim 13 wherein said accurate noise and/or
 2 interference value is applied to said look-up table, which computes a reciprocal

of said accurate noise and/or interference value to provide said normalization
4 factor.

16. The system of Claim 15 wherein said noise estimation circuit further
2 includes a multiplier for multiplying said scaled desired signal energy value by
said normalization factor to yield said accurate carrier signal-to-interference
4 ratio estimate.

17. The system of Claim 16 wherein said noise estimation circuit further
2 includes an averaging circuit for averaging said carrier signal-to-interference
ratio estimate and providing an averaged carrier signal-to-interference ratio
4 estimate in response thereto.

18. The system of Claim 17 further including a log likelihood ratio
2 circuit for computing a log likelihood ratio from said averaged carrier signal-to-
interference ratio estimate and path-combining weights scaled by said
4 normalization factor and averaged.

19. The system of Claim 11 wherein said noise estimation circuit
2 includes a subtractor for subtracting said desired signal component from said
pilot channel output and providing an interference signal in response thereto.

20. The system of Claim 19 wherein said noise estimation circuit
2 includes an energy computation circuit for providing said accurate noise
and/or interference value from said interference signal.

21. The system of Claim 1 further including means for computing
2 optimal path-combining weights for each multiple signal path comprising said
received signal.

22. The system of Claim 21 wherein said means for computing optimal
2 path-combining weights includes means for providing a scaled estimate of an
amplitude of said desired signal component from an output of a pilot filter and
4 a constant providing circuit, said scaled estimate normalized by said accurate
noise and/or interference value.

23. The system of Claim 22 wherein said scaled estimate is described by
2 the following equation:

$$\hat{\alpha} = \sqrt{\hat{E}_{s,l}} \cdot e^{j\hat{\theta}_l} / N_{t,l},$$

4 where $\hat{\alpha}$ is said scaled estimate; $\hat{E}_{s,l}$ is an estimate of a modulation symbol
energy of an l^{th} multipath component of said received signal; and $\hat{\theta}_l$ is an
6 estimate of a phase of said output of said pilot filter, and $N_{s,l}$ is said accurate
noise and/or interference value.

24. The system of Claim 23 further including a conjugation circuit for
2 providing a conjugate of said scaled estimate, said conjugate representative of
said optimal path-combining weights.

25. A system for providing an accurate interference value for a wireless
2 signal received over a channel comprising:

first means for measuring an interference component of said received
4 signal during a first time interval and providing an interference measurement
in response thereto;

6 second means for determining a fraction of said interference component
associated with signals transmitted during said first time interval and not to be
8 transmitted during a subsequent time interval; and

third means for adjusting said interference measurement by said fraction
10 and providing an adjusted noise measurement in response thereto as said
accurate interference energy value.

26. A method for reducing inaccuracies in measurements of noise
2 components of signals received over a channel comprising the steps of:
determining a multipath spread of said channel or an anticipated
4 multipath spread of said channel and
transmitting an idle skirt signal before and after transmitting a pilot
6 signal, said idle skirt signal having a length longer than said multipath spread
of said channel or an anticipated multipath spread of said channel.

27. A system for providing an accurate interference energy value for a
2 wireless signal received over a channel comprising:
a first receiver section for receiving said wireless signal and providing
4 in-phase and quadrature signal samples from said wireless signal in response
thereto;
6 a second receiver section for extracting a pilot signal from said in-phase
and quadrature signal samples and providing an estimate of an energy of said
8 wireless signal in response thereto, said estimate lacking an interference
component; and
10 an interference calculation circuit for providing said interference energy
value based on a measurement of a total energy of said wireless signal and said
12 estimate of an energy of said wireless signal.

28. A system for providing an accurate carrier signal-to-interference
2 ratio for facilitating the decoding of a signal received over a channel
comprising:
4 means for receiving a signal over a channel, said received signal having
one or more chips;
6 means for providing an estimate of total received energy per each of said
one or more chips, said estimate of total received energy having an interference
8 component and a desired signal energy component;
means for extracting from said received signal an estimate of said
10 desired signal energy component;

means for employing said estimate of said desired signal energy
12 component and said estimate of total received energy to provide an estimate
said interference component; and

14 means for using said estimate of said desired signal energy component
and said estimate of said interference component to provide said accurate
16 carrier signal-to-interference ratio.

29. A system for providing optimal inputs to a log-likelihood ratio
2 computation circuit comprising:

a first receiver section for receiving a signal over a channel;
4 an interference calculation circuit for providing a signal representative of
interference and/or noise contained in said signal and providing a signal-to-
6 interference ratio in response thereto;

an optimal path-combining circuit for employing said signal
8 representative of interference and/or noise and said signal to produce an
optimal path-combining signal as a first optimal input to said log-likelihood
10 ratio computation circuit; and

an accumulating circuit for accumulating said signal-to-interference ratio
12 to provide an optimal carrier signal-to-interference value as a second optimal
input to said log-likelihood ratio computation circuit.

30. A communications system comprising:

2 a transceiver for transmitting a first signal over a channel at a
predetermined rate and power level, said channel introducing noise and/or
4 interference to said first signal;

means for receiving said first signal and providing in-phase and
6 quadrature samples of said first signal in response thereto, said first signal
having a pilot signal component and one or more multipath components;

8 means for extracting said pilot signal and providing an estimate of total
interference energy received via said first signal on a predetermined multipath

10 component based on said pilot signal component and said in-phase and said
quadrature samples;

12 means for generating a power or rate control signal based on said
estimate of total interference energy and an estimate of energy associated with

14 said one or more multipath components;

means for transmitting said power or rate control signal to said

16 transceiver;

means for computing optimal path-combining weights for said one or

18 more multipath components based on said estimate of total interference energy
and providing optimally combined signal paths in response thereto;

20 means for computing a log-likelihood value based on said optimally
combined signal paths, said total interference energy, and said estimate of

22 energy associated with said one or more multipath components; and

means for decoding said first signal in response thereto.

31. A path weighting and combining circuit for determining maximal

2 ratio path-combining weights for multiple paths of a received signal that has an
interference component, a data component, and a pilot signal component

4 comprising:

a separating circuit for separating said pilot signal component and said

6 data component from said received signal;

a pilot filter for filtering said pilot signal to yield a filtered pilot signal;

8 an interference estimation circuit for estimating said interference
component and providing an interference value in response thereto;

10 a first multiplier for multiplying said filtered pilot signal by a
predetermined constant scaling factor and providing a scaled value in response

12 thereto;

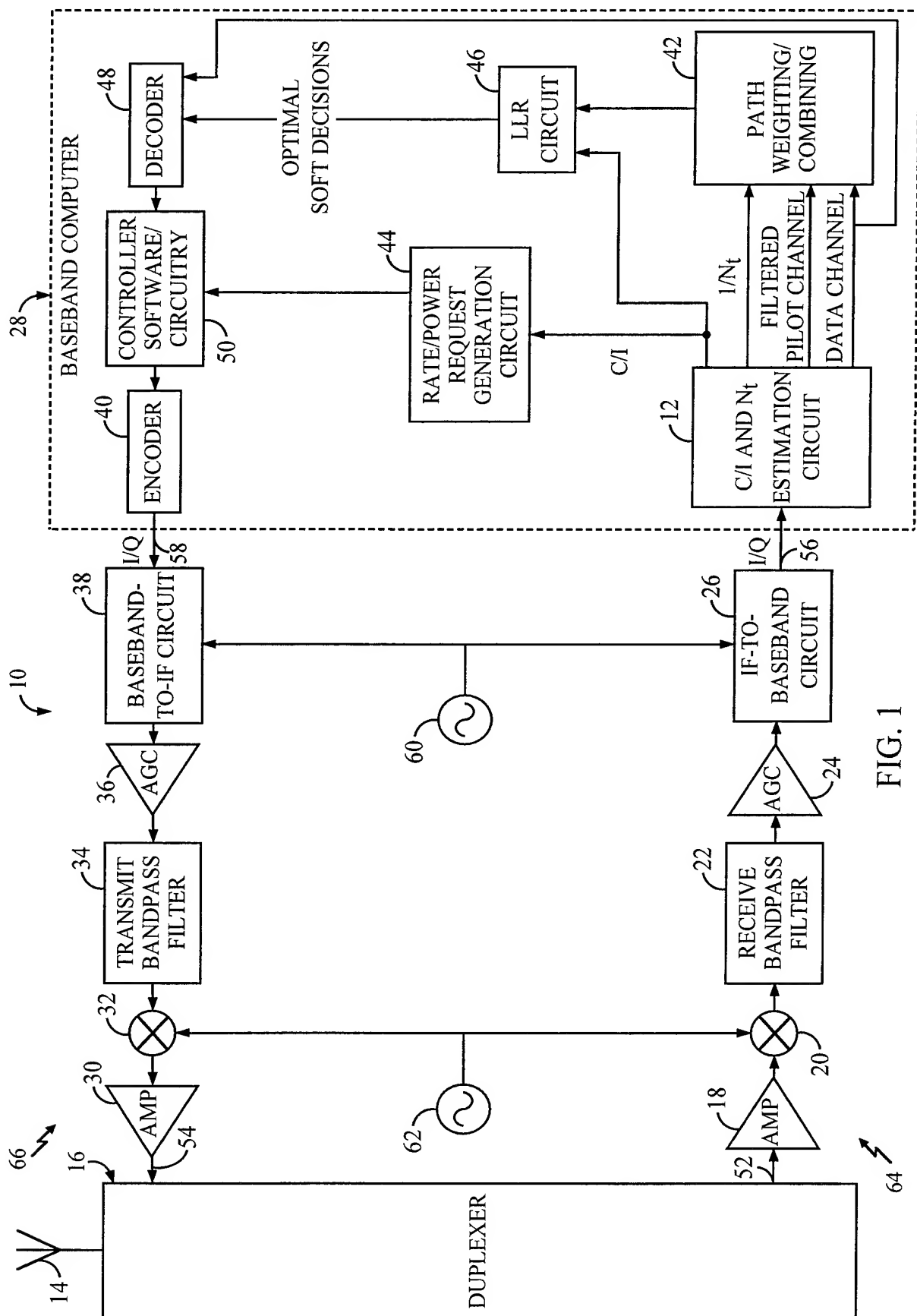
a second multiplier for multiplying said scaled value by a reciprocal of

14 said interference value to yield a weighted signal; and

a conjugation circuit for computing a conjugate of said weighted signal

16 to yield maximal ratio weights in response thereto.

32. A method for providing an accurate noise and/or interference value
2 for a signal received over a channel and transmitted by an external transceiver
comprising the steps of:
- 4 receiving said signal, said received signal having a desired signal
component and an interference and/or noise component;
- 6 extracting circuit for extracting an estimate of said desired signal
component from said received signal; and
- 8 providing said accurate noise and/or interference value based on said
estimate of said desired signal component and said received signal.



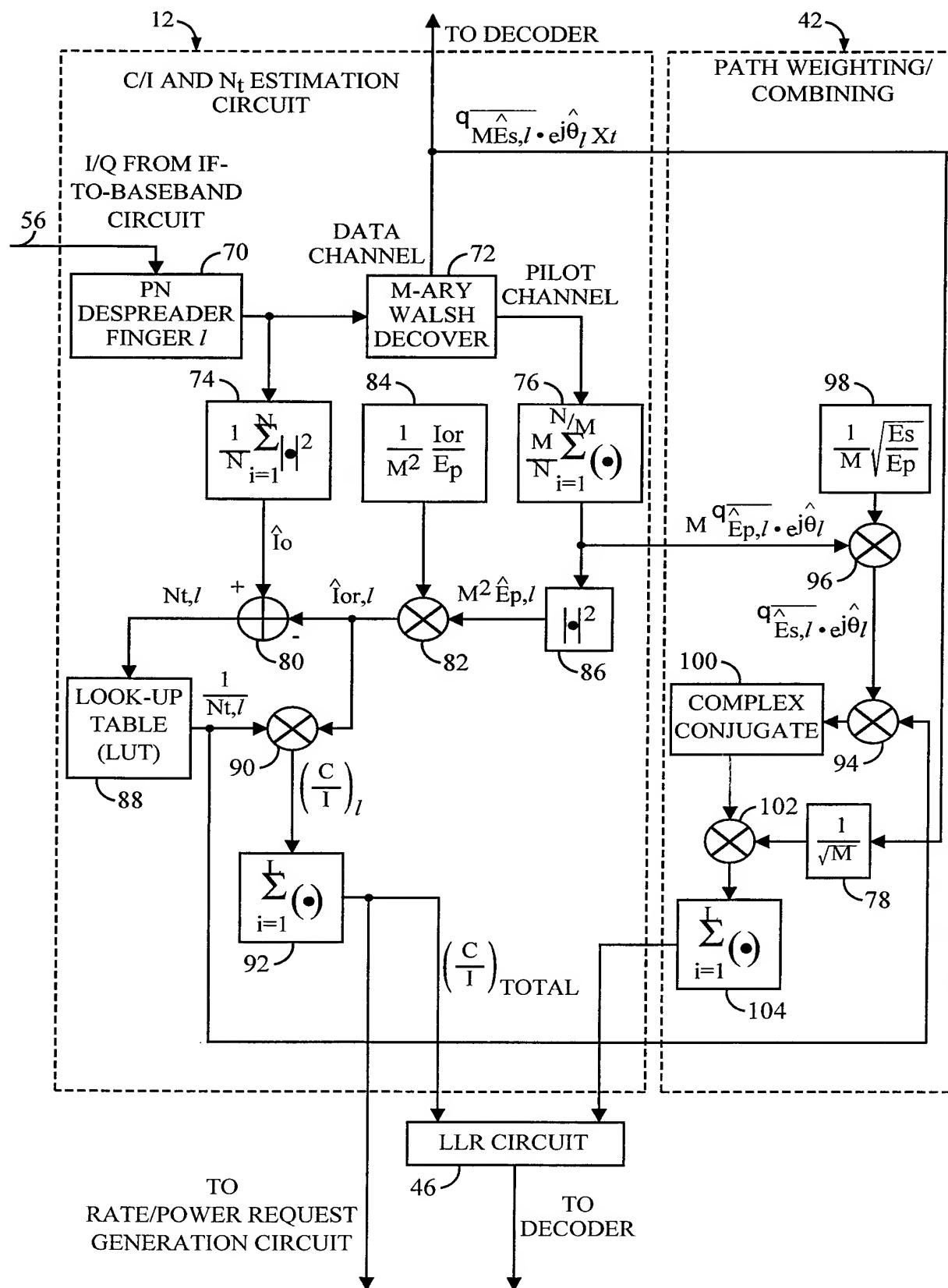
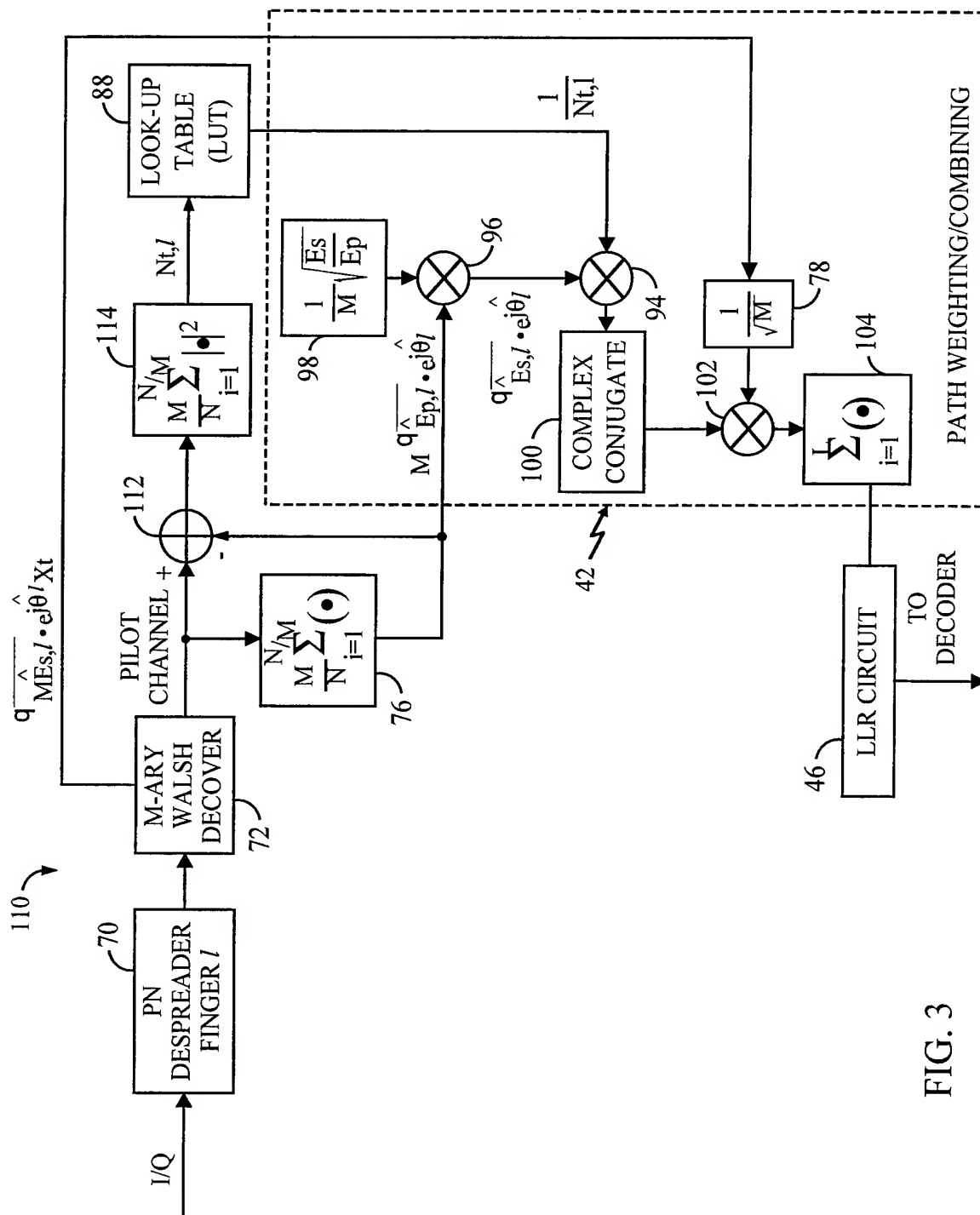


FIG. 2



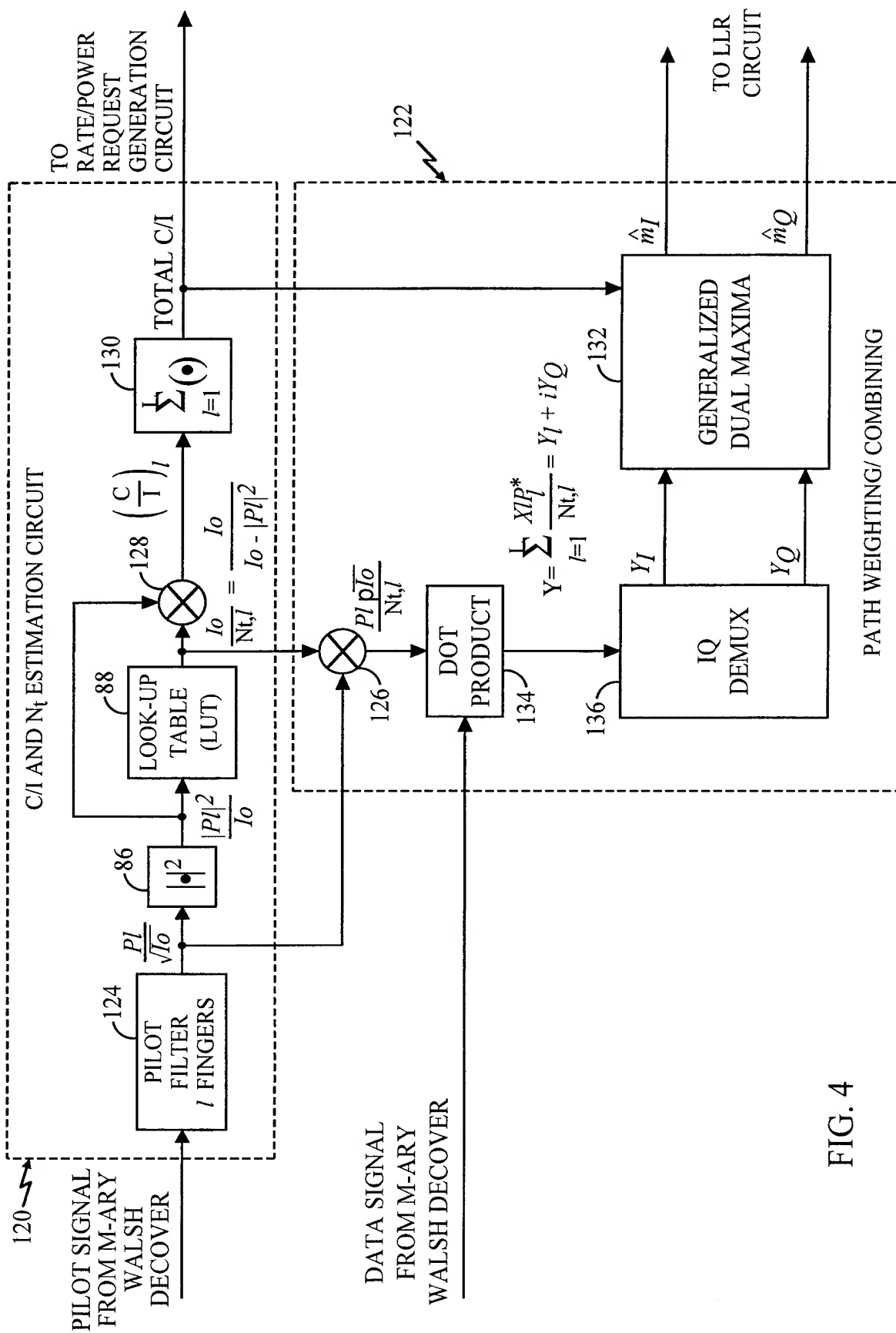


FIG. 4

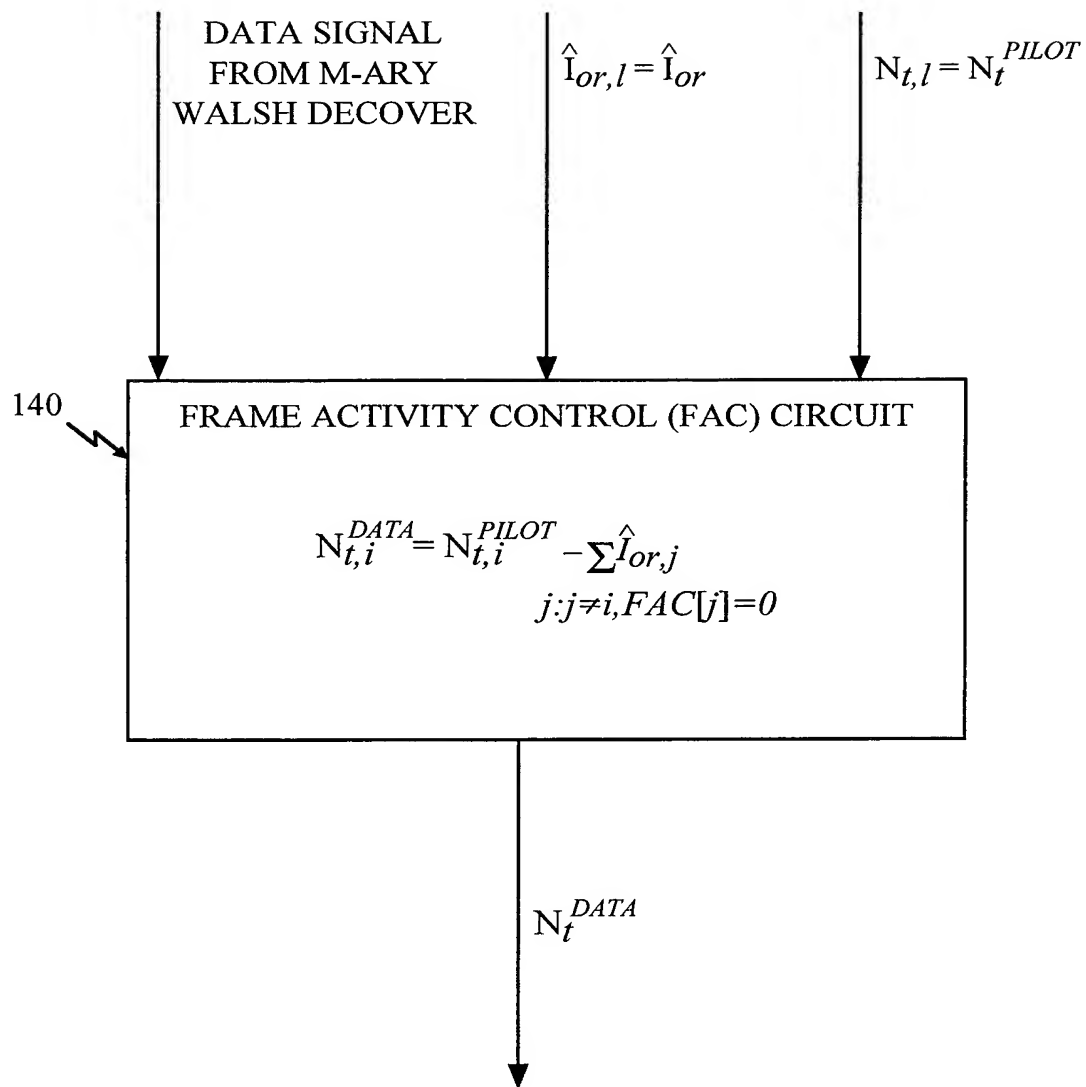


FIG. 5

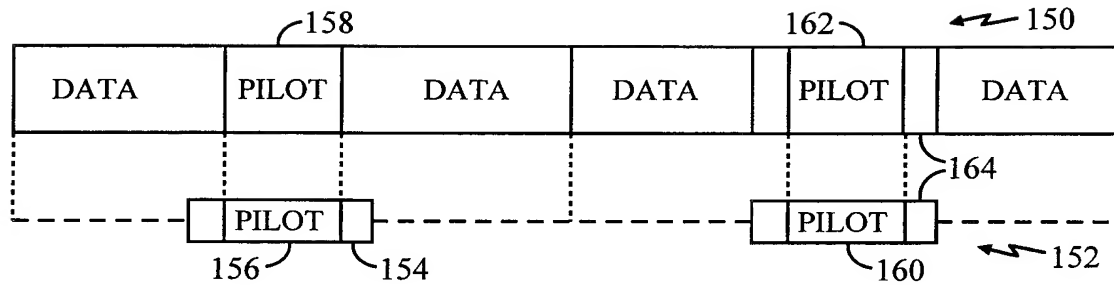


FIG. 6

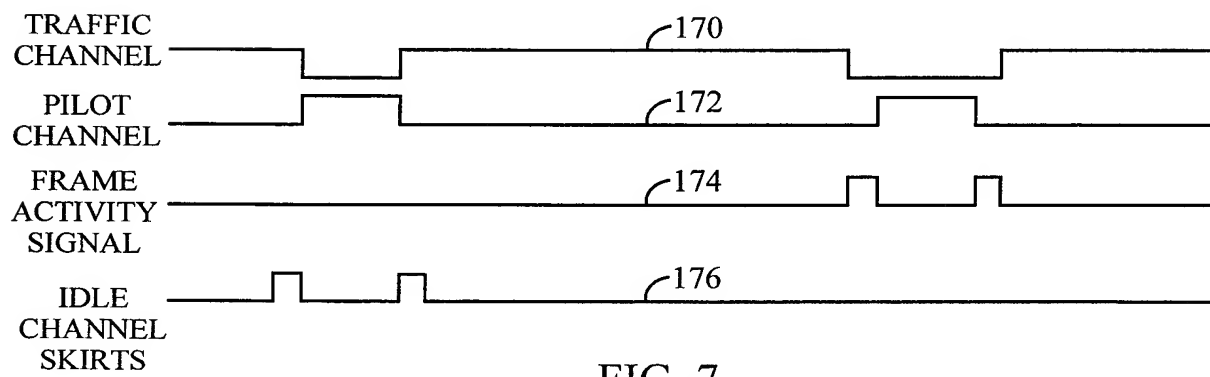


FIG. 7

INTERNATIONAL SEARCH REPORT

International Application No

PCT/US 00/12779

A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 H04B1/707

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 776 105 A (NIPPON TELEGRAPH & TELEPHONE) 28 May 1997 (1997-05-28) abstract column 5, line 55 -column 13, line 46 -----	1, 25, 27, 28, 30-32
A	WO 98 20617 A (QUALCOMM INC) 14 May 1998 (1998-05-14) abstract page 5, line 15 -page 6, line 30 -----	29

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

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Date of the actual completion of the international search

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